REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the application.

Disposition of Claims

Claims 4, 16, and 27 are pending in the present application. Claims 4, 16, and 27 are independent.

Rejection(s) Under 35 U.S.C § 103

Claims 4, 16, and 27 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,043,672 ("Sugasawara"). For the reasons set forth below, this rejection is respectfully traversed.

Embodiments disclosed in this application are directed to a method and apparatus for fault analysis of integrated circuits. In accordance with one embodiment shown in Figure 29, the integral transient power supply current measuring unit **1002** measures a transient power supply current generated by a test pattern sequence outputted by the test pattern sequence input unit **101** to take a time integral Q_{DDT} of the transient power supply current. The fault detector **1003** compares the time integral value Q_{DDT} measured by the measuring unit **1002** with a predetermined value to determine whether a delay fault is present or not in the analysis point of the circuit under test (*see* paragraph [0224] of the published specification).

Specifically, according to one embodiment, in deciding whether or not an open defect exists in an electronic circuit under test, such standards as whether or not a time integral value Q_{DDT} is over a predetermined value Q_{max} may be employed (*see* paragraph [0164] of the

published specification). Advantageously, embodiments disclosed in this application enable users to find whether an electronic circuit has an open defect and short circuit current in an analysis point by obtaining *a time integral of transient power supply current.*

Accordingly, independent claims 4, 16, and 27 require, in part, (i) the transient power supply current is determined to be abnormal when *time integral of the transient power supply current* is over a predetermined value. Further, independent claims 4, 16, and 27 require, in part, (ii) storing an analysis point included in said IC, the electric potential of which changes in accordance with changes of said supplied test pattern.

Sugasawara is directed to a test apparatus using selectable power supply lines for isolating defects in integrated circuits. Sugasawara suggests testing an IC based on quiescent current levels while a power supply line is divided into a plurality of parts.

With respect to Sugasawara, the Examiner has indicated on page 5 of the instant Office Action that Sugasawara discloses in col. 2, lines 38-41 that a transient power supply current is determined to be abnormal when time integral of the transient power supply current is over a predetermined value. However, it is noted that the indicated part of Sugasawara merely states that a failure analysis engineer seeks to determine which section of an integrated circuit is responsible for unusual current levels to isolate the defective area of the integrated circuit. As such, it is clear to one of ordinary skill in the art that Sugasawara is completely silent as to obtaining a time integral of a transient power supply current and comparing the time integral with a standard value to determine whether the analysis point is defective or not. Therefore, Sugasawara fails to teach or suggest the above limitation (i), as required by independent claims 4, 16, and 27.

In addition, as the Examiner has indicated on page 5 of the instant Office Action, Sugasawara also does not disclose (ii) storing an analysis point included in said IC, the electric potential of which changes in accordance with changes of said supplied test pattern, as required by independent claims 4, 16, and 27.

In view of the above, Sugasawara fails to disclose at least the limitations (i) and (ii), as required by independent claims 4, 16, and 27. Claims 4, 16, and 27 are therefore patentable over Sugasawara. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 02008/071003).

Dated: November 26, 2007

Respectfully submitted,

By _____

Thomas K. Scherer
Registration No.: 45,079
OSHA · LIANG LLP
1221 McKinney St., Suite 2800
Houston, Texas 77010
(713) 228-8600
(713) 228-8778 (Fax)
Attorney for Applicant

Attachments